Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	19	(via with Alcu) and barrier and (multi with (level or layer or interconnects or metallurgy or metal or conductive))	US-PGPUB; USPAT	OR	ON	2005/06/09 14:26
L2	18	1 and @ad<"20040330"	US-PGPUB; USPAT	OR	ON	2005/06/09 14:27
L3	49	(via same Alcu) and barrier and (multi with (level or layer or interconnects or metallurgy or metal or conductive))	US-PGPUB; USPAT	OR	ON	2005/06/09 14:49
L4	47	3 and @ad<"20040330"	US-PGPUB; USPAT	OR	ON	2005/06/09 14:50
L5	29	4 not 2	US-PGPUB; USPAT	OR	ON	2005/06/09 14:52
L6	0	(via same Alcu) and barrier and (multi with (level or layer or interconnects or metallurgy or metal or conductive))	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/09 14:35
L7	11	(via same Alcu) and barrier and (multi with metallization)	US-PGPUB; USPAT	OR	ON	2005/06/09 14:51
L8	11	7 and @ad<"20040330"	US-PGPUB; USPAT	OR	ON	2005/06/09 14:52
L9	5	8 not 2	US-PGPUB; USPAT	OR	ON	2005/06/09 14:50
L10	0	(via same Alcu) and barrier and (multi with metallization)	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/09 14:51
L11	0	(via same CuAl) and barrier and (multi with metallization)	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/09 14:51
L12	0	(via same CuAl) and barrier and (multi with metallization)	US-PGPUB; USPAT	OR	ON	2005/06/09 14:51
L13	56	(via same (Cu with Al)) and barrier and (multi with metallization)	US-PGPUB; USPAT	OR	ON	2005/06/09 14:51
L14	54	13 and @ad<"20040330"	US-PGPUB; USPAT	OR	ON	2005/06/09 14:52
L15	51	14 not 2	US-PGPUB; USPAT	OR	ON	2005/06/09 14:52
L16	48	15 not 8	US-PGPUB; USPAT	OR	ON	2005/06/09 14:52
L17	48	16 not 5	US-PGPUB; USPAT	OR	ON	2005/06/09 14:52

US-PAT-NO: 6638795

DOCUMENT-IDENTIFIER: US 6638795 B2

TITLE: Semiconductor device and method of fabricating the same

---------- KWIC ---------

Brief Summary Text - BSTX (7):
Recently, as the degree of integration of semiconductor elements increases and the chip size decreases, the microfabrication of **interconnects** and the formation of **multi-level interconnects** are advancing acceleratedly. In a logic device having this **multi-level interconnect,** a wiring delay is becoming one dominant cause of a device signal delay. The device signal delay is proportional to the product of the wiring resistance and the wiring capacitance. Accordingly, it is important to reduce the wiring resistance and the wiring capacitance in order to reduce the wiring delay.

Detailed Description Text - DETX (4):
The first embodiment will be described below. In this embodiment, a semiconductor device including a wiring structure having a Cu **multi-level interconnect** and a redundancy fuse, as the main constituent elements of the present invention, and a method of fabricating the same will be explained. For the sake of convenience, the structure of the semiconductor device will be explained along with its fabrication method.

Detailed Description Text - DETX (17):
As shown in FIG. 2B, a TaN **barrier** metal film 20 about 25 nm thick and a Cu film 21 about 200 nm thick as a seed metal film are successively deposited in a vacuum by using a clustered sputtering apparatus. In this step, the RF processing and the formation of the **barrier** metal film 20 and the Cu film 21 are desirably successively performed in a vacuum.

Detailed Description Text - DETX (18):
As shown in FIG. 2C, the **barrier** metal 20 is used as an electrode to form, by plating, a Cu film 22 having a film thickness, about 1 .mu.m in this embodiment, by which the first wiring trenches 19 are filled.

Detailed Description Text - DETX (19):
Subsequently, as shown in FIG. 3A, to separate the Cu film 22 by the

damascene process, the Cu film 22 (21) and the **barrier** metal film 20 are polished by CMP to leave the Cu film 22 only in the first wiring trenches 19, forming first interconnects 23.

Detailed Description Text - DETX (20):

As shown in FIG. 3B, an Si.sub.3 N.sub.4 film 24 about 70 nm thick serving as a diffusion **barrier** (passivation) on the surfaces of the first interconnects 23 is deposited. Next, on this Si.sub.3 N.sub.4 film 24, an FSG dielectric interlayer 25 about 700 nm thick, an Si.sub.3 N.sub.4 film 26 about 30 nm thick, and another FSG dielectric interlayer 27 about 700 nm thick are formed in this order, and an antireflection film 28 is also formed.

Detailed Description Text - DETX (26):

As shown in FIG. 6A, a TaN **barrier** metal film 34 about 25 nm thick and a Cu film 21 about 200 nm thick as a seed metal film are successively deposited in a vacuum by using a sputtering apparatus. The **barrier** metal 34 is used as an electrode to form, by plating, a Cu film 35 having a film thickness, about 1 .mu.m in this embodiment, by which the second wiring trenches 33 and the via holes 30 are filled.

Detailed Description Text - DETX (27):

Subsequently, as shown in FIG. 6B, to separate the Cu film 35 by the damascene process, the Cu film 35 and the **barrier** metal film 34 are polished by CMP to leave the Cu film 35 only in the second wiring trenches 35 and the via holes 30. After that, the resultant structure is cleaned by the wet process to form second interconnects 36, thereby completing a lower wiring layer including the first interconnects 23 and the second interconnects 36.

Detailed Description Text - DETX (28):

As shown in FIG. 7A, an Si.sub.3 N.sub.4 film 37 about 100 nm thick serving as a diffusion **barrier** (passivation) on the surfaces of the second interconnects 36 is deposited. After that, an SiO.sub.2 film 38 about 1 .mu.m thick is formed as a dielectric interlayer.

Detailed Description Text - DETX (31):

While the vacuum state when the TiN film 43 is formed is kept, a Cu alloy, in this embodiment a **Cu--Al** alloy film 44, is deposited by sputtering so as to fill the third wiring trenches 39 and the **via** holes 45. The Al addition amount of this Cu--Al alloy film 44 is preferably a value within the range of 1 to 10 atm %, since a large addition amount by which a metal oxide film to be described later can be reliably formed is necessary when a redundancy fuse is cut.

Detailed Description Text - DETX (33):

Subsequently, as shown in FIG. 8B, another TiN film 43 about 100 nm film is deposited by sputtering so as to cover the upper surface of the Cu--Al alloy film 44, and the SiO.sub.2 film 38 is used as a stopper to polish this TiN film 43 by CMP. Consequently, in the fuse region 41, a redundancy fuse 51 is formed which fills the third wiring trench 39 and the **via** hole 45 and consists of the TiN film 43 and the **Cu--Al** alloy film 44 entirely surrounded by the TiN film 43. In the wiring region 42, an upper wiring layer 52 is formed which similarly consists of the TiN film 43 and the Cu--Al alloy film 44 entirely surrounded by the TiN film 43.

Detailed Description Text - DETX (61):

In this embodiment, as in the first embodiment, a semiconductor device including a wiring structure having a Cu **multi-level interconnect** and a redundancy fuse and a method of fabricating the same will be explained. The second embodiment differs from the first embodiment in that the steps of fabricating the redundancy fuse are slightly different.

Detailed Description Text - DETX (64):

As shown in FIG. 17A, an Si.sub.3 N.sub.4 film 37 about 100 nm thick serving as a diffusion **barrier** (passivation) on the surfaces of the second interconnects 36 is deposited. After that, an SiO.sub.2 film 38 about 2 .mu.m thick is formed as a dielectric interlayer, and the surface layer of this SiO.sub.2 film 38 is planarized by CMP until the film thickness becomes about 1 .mu.m.

Detailed Description Text - DETX (70):

Consequently, as shown in FIG. 18B, the right-hand region forms a fuse region 41, and the left-hand region forms a wiring region 42. In the fuse region 41, a redundancy fuse 71 is formed which fills the **via** hole 45 and consists of the TiN films 43 and the **Cu--Al** alloy film 44 vertically sandwiched by these TiN films 43. In the wiring region 42, an upper wiring layer 72 is formed which similarly consists of the TiN films 43 and the Cu--Al alloy film 44 vertically sandwiched by these TiN films 43.

DOCUMENT-IDENTIFIER: US 20030183913 A1

TITLE: Method of eliminating back-end rerouting in ball grid array packaging

---------- KWIC ---------

Detail Description Paragraph - DETX (7):

[0036] Referring to FIG. 2, the last Cu layer 8 is covered with a silicon nitride 9 and a silicon oxide 13 layer like in the prior art. A contact hole (**via**) is defined by lithography and etched into oxide and nitride to provide electrical contact to the last metal level 6 which is an aluminum copper alloy (**AlCu**). Afterwards a passivation consisting of an oxide layer 11 and nitride layer 12 is deposited. Other known passivation layers may alternatively be used, such as borosilicate glass (BSG). On top of the passivation a photosensitive poly-imide 4 is deposited, exposed and developed. A large terminal via is etched into the nitride 12 and oxide 11 stopping on top of the oxide layer 13. It has to be considered, that all of the material deposited into the **vias** will be removed to allow the **AlCu** alloy to contact the Cu (dual-) damascene layer.

DOCUMENT-IDENTIFIER: US 20030134464 A1

TITLE: Semiconductor device and method for the manufacture thereof

---------- KWIC ---------

Detail Description Paragraph - DETX (138):

[0273] The process of manufacturing the semiconductor device according to the seventh embodiment is characterized in that at least one of the materials, Al, **AlCu,** AlCuSi, WSi.sub.2, and Cu (aluminum in this embodiment) is made to reflow in order to fill up **via** holes for performing the connection of the second layer wiring (bit line or another wiring) in a two-layer wiring structure.

Detail Description Paragraph - DETX (147):

[0282] In a third insulation layer 30 which covers the upper surface of the substrate containing the respective wirings mentioned above and the surface of which is flattened, via holes are selectively formed corresponding to and positioned above the bit line buried plug connection wirings 36 and the first layer wiring 37. Further, at least one (aluminum in this embodiment) of the materials, Al, **AlCu,** AlCuSi, Wsi.sub.2 and Cu, is made to reflow so as to fill up the interiors of the **via** holes. A bit line BL connected to the bit line buried plug connection wiring 36 through the via hole portion and a second layer wiring 38 connected to the first wiring 37 through the via hole portion are formed. Further, a passivation film 39 is formed, and in a pad portion, a hole is bored.

Detail Description Paragraph - DETX (148):

[0283] As for the manufacture of the memory cells which each have an information storage capacitor using a ferroelectric film composed of a material having the perofskite structure or the lamellar perofskite structure and a switching transistor as mentioned above and the ferroelectric memory having a multi-wiring structure consisting of more than two layers, there is used the step of reflowing one (aluminum in this embodiment) of the materials, Al, **AlCu,** AlCuSi, WSi.sub.2, and Cu, in order to fill up the **via** holes in the multi-layer structure at the bit line forming step.

DOCUMENT-IDENTIFIER: US 20030074789 A1

TITLE: MODIFIED PAD FOR COPPER/LOW-K

---------- KWIC ---------

Detail Description Paragraph - DETX (18):

[0026] As shown in FIG. 3, patterned masking layer 34 is formed over **AlCu** bonding pad layer 34 (and TiN barrier layer 30) to additionally mask a portion of **AlCu** bonding pad layer 34 that overlies a peripheral planar area 36 over substrate/die 12 that does not have the metal **vias** 18 thereunder.

Detail Description Paragraph - DETX (21):

[0028] As shown in FIG. 4, in a key step of the invention, AlCu bonding pad layer 32 and TiN barrier layer 30 are etched, using patterned masking layer 34 as a mask, to form extended, permanent, AlCu bonding pad 32' with underlying extended, permanent, TiN barrier layer 30'. Extended **AlCu** bonding pad 32', with underlying extended TiN barrier layer 30', extend over peripheral planar area 36 of substrate/die 12 that does not have the metal **vias** 18 thereunder.

Detail Description Paragraph - DETX (24):

[0030] Wire bond 40, including wire 42 that is preferably comprised of gold (Au), is permanently attached/affixed to extended **AlCu** bonding pad 32' at peripheral planar area 36 over substrate/die 12 that does not have the metal **vias** 18 thereunder. The inventors have determined that such a wire bond 40 arrangement does not cause cracking of low-k dielectric layer 20, or peeling of: (1) AlCu bonding pad 32' with underlying extended TiN barrier layer 30'; and/or (2) SiON/SiN etch stop layer 22 from low-k dielectric layer 20. In the conventional pad structure, the wire bonding will fail at the via bottom (18) due to low mechanical properties and bad heat transport.

Detail Description Paragraph - DETX (25):

[0031] It is noted that a conventional bonding pad structure would not include permanent extended **AlCu** bonding pad 32' over peripheral planar area 36, and would instead affix wire bond 40 to portion 50 of non-extended **AlCu** bonding pad over metal **vias** 18. As noted above, the inventors have determined that such a conventional bonding pad structure is highly susceptible to cracking of the low-k dielectric layer, and/or peeling of: the bonding pad; and/or the etch stop layer from the low-k dielectric layer.

US-PAT-NO: 6593230

DOCUMENT-IDENTIFIER: US 6593230 B1

TITLE: Method of manufacturing semiconductor device

---------- KWIC ---------

Brief Summary Text - BSTX (7):

For example, in a case where inter-wiring-layer **via** holes are formed, through conventional dry etching, when underlying wiring layers 16a, 16b include **AlCu** films 10a, 10b, Ti films 12a, 12b and TiN films 14a, 14b, a **via** hole 20a in which both the TiN film 14a and the Ti film 12a of the underlying wiring layer 16a are etched through to the bottom thereof and a **via** hole 20b in which the TiN film 14b and the Ti film 12b of the underlying wiring layer 16b remain are formed above the same substrate 2 depending on thickness of a planarized interlayer film 18. In particular, in the **via** hole 20a in which the TiN film 14a and the Ti film 12a are etched through to the bottom thereof, Al of the **AlCu** film 10a of the underlying wiring layer 16a reacts to a gas of a CF family which is an etchant, and a low-volatile fluoride 22 is formed and is deposited on the sidewall of the **via** hole 20a. The fluoride 22 increases the contact resistance of the via hole 20a and increases variation of the resistance value. Further, during a degassing process on the order of 500.degree. C. performed before an upper wiring layer is formed, Al of the **AlCu** film 10a, exposed at the bottom of the **via** hole 20a as a result of the TiN film 14a and the Ti film 12a being etched through to the bottom thereof, may blow out, and, as a result, short-circuiting between wiring patterns may occur.

Detailed Description Text - DETX (5):

With reference to FIG. 2A, on a single-crystal silicon substrate 26, in an active area isolated by device-isolating regions 28, a gate electrode 32 is formed via a gate oxide film, and source-drain diffusion layers 30 are formed through an ion implantation process or the like. Then, an interlayer insulating film 34 is formed on the silicon substrate 26. Then, contact holes 36a, 36b are formed above the gate electrode 32 and the source-drain diffusion layer 30, respectively. Then, a barrier layer is deposited through sputtering on the entire surface of the silicon substrate 26. Then, from the bottom, sequentially in the below-stated order, for example, 500 nm of an AlCu film, 20 nm of a Ti film, and 50 nm of a TiN film are deposited through sputtering, and patterned. As a result, on the contact holes 36a, 36b, lower (first) wiring

layers 46a, 46b including the **AlCu** films 40a, 40b, Ti films 42a, 42b and TiN films 44a, 44b are formed **via the barrier** layers 38a, 38b.

Detailed Description Text - DETX (13):

When the second etching is started, the thickness of the bottom film 48 remaining below the pattern 56a is approximately equal to the thickness of the bottom film 48 remaining below the pattern 56b. As a result, the time required for etching the remaining bottom film 48 to the bottom thereof below the pattern 56a is approximately the same as the time required for etching the remaining bottom film 48 to the bottom thereof below the pattern 56b. In actuality, before the bottom film 48 is etched through to the bottom thereof below the pattern 56b, the bottom film 48 is etched through to the bottom thereof below the pattern 56a and the TiN film 44a starts being etched below the pattern 56a. However, in the condition under which the second etching is performed, the etching rate for the TiN film 44a is approximately 1/12 of the etching rate for the bottom film 48. Therefore, merely a slight depth of the TiN film 44a is etched below the pattern 56a when the bottom film 48 is etched through to the bottom thereof below the pattern 56b. As a result, without causing the TiN films 44a, 44b below the pattern 56a, 56b to be passed through so that the Ti films 42a and 42b and **AlCu** films 40a, 40b below the TiN films 44a, 44b are exposed, the bottom film 48 can be etched through to the bottom thereof below the patterns 56a and 56b, and, thus, the **via** holes 58a and 58b can be formed above the first wiring layers 46a, 46b. Then, the photoresist 54 is removed. Thus, the structure shown in FIG. 2D is obtained.

Detailed Description Text - DETX (14):

Then, 20 nm of a Ti film, 500 nm of an AlCu film, 20 nm of a Ti film and 50 nm of a TiN film are deposited through sputtering, in the stated order, on the top film 52, and are patterned. As a result, above the **via** holes 58a, 58b, the second wiring layers 76a, 76b including the Ti films 68a, 68b, the **AlCu** films 70a, 70b, the Ti films 72a, 72b and the TiN films 74a, 74b are formed, as shown in FIG. 2E. As shown in the figure, the Ti films 68a, 68b are formed on the bottom and the sidewall of the **via** holes 58a, 58b, respectively, and the **via** holes 58a, 58b are filled with **AlCu** 70a, 70b, respectively. Thus, the first wiring layers 46a, 46b are electrically connected with the second wiring layers 76a, 76b, respectively.

US-PAT-NO: 6159842

DOCUMENT-IDENTIFIER: US 6159842 A

TITLE: Method for fabricating a hybrid low-dielectric-constant intermetal dielectric (IMD) layer with improved reliability for multilevel interconnections

---------- KWIC ---------

Brief Summary Text - BSTX (13):

In accordance with the objects of this invention, a new method is achieved for fabricating a hybrid low-dielectric constant IMD layer on a semiconductor substrate having semiconductor devices and an overlying insulating layer. A conductive layer is deposited on the insulating layer. The conductive layer is patterned to form a first level of interconnecting lines to the devices on the substrate. The conductive layer is typically a metal, such as aluminum/copper (**AlCu**). A conformal insulating layer, such as silicon oxide (SiO.sub.2), and more specifically a low-k silicate material composed of fluorine-doped silicon glass (**FSG**) having a dielectric constant of about 3.5, is deposited to protect the patterned conductive layer. Next, a porous first low-k material, and having an even lower dielectric constant (k), for example, less than 3.0, is deposited between the interconnecting metal lines, but not over the metal lines. The porous low-k layer, such as hydrogen silsesquioxane (HSQ) having a dielectric constant k (about 3), provides an insulating layer that minimizes the intralevel capacitance. A denser second low-k material, for example composed of fluorine-doped silicon glass (**FSG**), is deposited over the electrical interconnecting lines and over the porous first low-k material to form a cap layer that protects the porous first low-k material and concurrently to minimize interlevel capacitance. This completes the hybrid low-dielectric constant intermetal dielectric (IMD) layer for the first level of metal interconnections. Next, additional levels of hybrid low-k IMD layers can be formed by etching via holes in the second low-k layer and the insulating layer to the first level of interconnecting metal lines and forming metal plugs. The above method is then repeated for each additional level of metal interconnections necessary for wiring up the integrated circuit.

US-PAT-NO: 6376353

DOCUMENT-IDENTIFIER: US 6376353 B1

TITLE: Aluminum and copper bimetallic bond pad scheme for copper damascene interconnects

---------- KWIC ---------

Brief Summary Text - BSTX (20):

The processes of the present invention fabricate Al--Cu wire bonding pads that have good adhesion properties (no metal interface separation/peel failures or interface fracture failures). Since there are a large statistical number of these structures, failure rates are very low and show a high reliability, as tested by gold wire bond pull tests. **Temperature** and humidity cycling tests also indicate the robustness of the processes of this invention, free from stress-crack corrosion, peeling, interface failure, adhesion failures.

Detailed Description Text - DETX (12):

Referring to FIG. 3b, illustrated in cross-sectional drawing, provided is a continuation of the processing described above in FIG. 3a, describing the first embodiment of the present invention. Selective wet etching of the top layer of copper 20 is performed by a DMSO/CCl.sub.4 solution, dimethylsulfoxide, carbon tetrachloride. This wet etching step yields a recessed top metal copper layer 24. Some of the process details and specifications for this etching step, are as follows. The etch solutions is DMSO/CCl.sub.4 solution, dimethylsulfoxide, carbon tetrachloride, in a **temperature** range between 20 to 150.degree. C., for an etch rate range between 5 to 100 Angstroms per minute, in an etch time of between 1 to 60 minutes, for a copper removal between about 100 to 8000 Angstroms. Other chemical solutions for this wet etching step include one or more of the following group, consisting of hydrofluoric acid (HF), acetic acid (CH.sub.3 COOH), ammonium fluoride (NH.sub.4 F), tetramethylammonium hydroxide (TMAH), tetraethylammonium hydroxide (TEAH), tetrapropylammonium hydroxide (TPAH), benzotriazole, surfactant and water. The preferred etch solution mixtures include: NH.sub.4 F/CH.sub.3 COOH, HF/NH.sub.4 F/H.sub.2 O, HF/NH.sub.4 F/H.sub.2 O/surfactant, and TMAH/H.sub.2 O.

Detailed Description Text - DETX (23):

A summary of some of the processing details and specifications for Al--Cu alloy metal, that forms the Al--Cu bond pad layer, follow, and these process

details apply to all the embodiments of the present invention, described earlier. For deposition of the Al--Cu or Al--Cu alloy metal by physical vapor deposition (PVD), the following sputtering conditions are: DC Magnetron sputtering with argon gas at **pressures** between about 0.1 to 10,000 mTorr, DC power from about 100 to 10,000 Watts, wafer **temperature** from about 25 to 500.degree. C., argon gas flows from about 0.1 to 100 sccm. Following the Al--Cu deposition, an annealing step follows to enhance Al--Cu alloy formation. The annealing process details follow: gas ambient is a mixture of nitrogen and hydrogen gas or forming gas, **temperature** between about 200 to 500.degree. C. at anneal times from about 20 to 60 minutes, and **pressures** between about 400 to 760 Torr (atmosphere).

Detailed Description Text - DETX (24):

Note, for good bond pad metallurgy in dual copper damascene processing, both pure metals, aluminum and copper, have the same face centered cubic (fcc) crystal structure and are close in atomic metallic radii size (coordination 12), for good, solid-solid solubility. Also, good electrical conductivity is good for both Cu and Al, Cu=0.94 and Al=0.50 (micro-Ohms).sup.-1, respectively, with almost a 2.times. factor better conductivity for pure copper than for pure aluminum. Therefore, copper rich alloys are better than aluminum rich alloys for conductivity. All equilibrium and non-equilibrium crystal structure phases in the aluminum copper phase diagram are possible from 0 to 100 weight percent (0 to 100 atomic percent) in the Al--Cu alloy layer, depending on the composition and **temperature** treatments, for good solid-solid state solution formation.

Detailed Description Text - DETX (26):

The processes of the present invention fabricate Al--Cu wire bonding pads that have good adhesion properties (no metal interface separation/peel failures or interface fracture failures). Since there are a large statistical number of these structures, failure rates must be very low and reliability very high, as tested by gold wire bond pull tests. **Temperature** and humidity cycling tests indicate the robustness of the process and structure from stress-crack corrosion, peeling, interface failure, adhesion failures.

Claims Text - CLTX (23):

7. The method of claim 1, wherein the top layer of copper within the trench/via, forming recessed copper within the trench/via, is etched back selectively by wet etch using DMSO/CCl.sub.4 solution, dimethylsulfoxide, carbon tetrachloride, in a **temperature** range from 20 to 150.degree. C., for an etch rate range between 5 to 100 Angstroms per minute, in an etch time of between 1 to 60 minutes, for a copper removal between about 100 to 8000

Angstroms.

Claims Text - CLTX (28):
12. The method of claim 1, wherein a blanket layer of **AlCu** alloy metal is deposited over said second barrier layer by physical vapor deposition (PVD), **sputtering,** for a film thickness from about 2,000 to 20,000 Angstroms, using the following process conditions: DC **Magnetron sputtering** with argon gas at **pressures** between about 0.1 to 10,000 mTorr, DC power from about 100 to 10,000 Watts, wafer **temperature** from about 25 to 500.degree. C., argon gas flows from about 0.1 to 100 sccm.

Claims Text - CLTX (29):
13. The method of claim 1, wherein the forming gas annealing the layer of Al--Cu alloy, enhancing alloy formation, consists of the following conditions: gas ambient is a mixture of nitrogen and hydrogen gas or forming gas, **temperature** between about 200 to 500.degree. C. at anneal times from about 20 to 60 minutes, and **pressures** between about 400 to 760 Torr (atmosphere).

Claims Text - CLTX (64):
29. The method of claim 19, wherein a blanket layer of **AlCu** alloy metal is deposited over said second barrier layer by physical vapor deposition (PVD), **sputtering,** for a film thickness from about 2,000 to 20,000 Angstroms, using the following process conditions: DC **Magnetron sputtering** with argon gas at **pressures** between about 0.1 to 10,000 mTorr, DC power from about 100 to 10,000 Watts, wafer **temperature** from about 25 to 500.degree. C., argon gas flows from about 0.1 to 100 sccm.

Claims Text - CLTX (65):
30. The method of claim 19, wherein the forming gas annealing the layer of Al--Cu alloy, enhancing alloy formation, consists of the following conditions: gas ambient is a mixture of nitrogen and hydrogen gas or forming gas, **temperature** between about 200 to 500.degree. C. at anneal times from about 20 to 60 minutes, and **pressures** between about 400 to 760 Torr (atmosphere).

Claims Text - CLTX (101):
46. The method of claim 36, wherein a blanket layer of **AlCu** alloy metal is deposited over said second barrier layer by physical vapor deposition (PVD), **sputtering,** for a film thickness from about 2,000 to 20,000 Angstroms, using the following process conditions: DC **Magnetron sputtering** with argon gas at **pressures** between about 0.1 to 10,000 mTorr, DC power from about 100 to 10,000 Watts, wafer **temperature** from about 25 to 500.degree. C., argon gas flows from about 0.1 to 100 sccm.

Claims Text - CLTX (102):

47. The method of claim 36, wherein the forming gas annealing the layer of Al--Cu alloy, enhancing alloy formation, consists of the following conditions: gas ambient is a mixture of nitrogen and hydrogen gas or forming gas, **temperature** between about 200 to 500.degree. C. at anneal times from about 20 to 60 minutes, and **pressures** between about 400 to 760 Torr (atmosphere).

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	8	(magnetron with sputtering) with AlCu	US-PGPUB; USPAT	OR	ON	2005/06/09 16:17
L2	3	1 and temperature and pressure	US-PGPUB; USPAT	OR	ON	2005/06/09 17:06
L3	1	(AlCu with FSG)	US-PGPUB; USPAT	OR	ON	2005/06/09 17:07
L4	12	(AlCu same FSG)	US-PGPUB; USPAT	OR	ON	2005/06/09 17:07

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	506	via with (Al near Cu)	US-PGPUB; USPAT	OR	ON	2005/06/09 11:36
L2	84	1 and (multi with (level or interconnect))	US-PGPUB; USPAT	OR	ON	2005/06/09 11:36
L3	76	2 and @ad<"20040330"	US-PGPUB; USPAT	OR	ON	2005/06/09 11:26
L4	58	3 and barrier	US-PGPUB; USPAT	OR	ON	2005/06/09 11:26
L5	87	via with (Al near Cu)	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/09 11:36
L6	0	5 and (multi with (level or interconnect))	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/09 11:36

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	8	(magnetron with sputtering) with AlCu	US-PGPUB; USPAT	OR	ON	2005/06/09 16:17
L2	3	1 and temperature and pressure	US-PGPUB; USPAT	OR	ON	2005/06/09 17:06
L3	1	(AlCu with FSG)	US-PGPUB; USPAT	OR	ON	2005/06/09 17:07
L4	12	(AlCu same FSG)	US-PGPUB; USPAT	OR	ON	2005/06/09 17:07
L5	151	silicide and CMOS and AlCu	US-PGPUB; USPAT	OR	ON	2005/06/09 17:34
L6	146	5 and @ad<"20040330"	US-PGPUB; USPAT	OR	ON	2005/06/09 17:34